

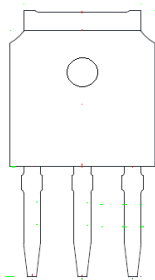
GENERAL DESCRIPTION

The MEE4294P2-G is a N-Channel enhancement mode power field effect transistor, using Force-MOS patented Extended Trench Gate (ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

PIN CONFIGURATION

(TO-251)

Top View

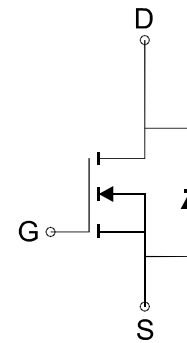


FEATURES

- $R_{DS(ON)} \leq 10.5m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 16.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- Synchronous Rectification
- Load Switch



N-Channel MOSFET

Ordering Information: MEE4294P2-G (Green product- Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current*	I_D	$T_C=25^\circ C$	35
		$T_C=70^\circ C$	28
		$T_A=25^\circ C$	11
		$T_A=70^\circ C$	9
Pulsed Drain Current	I_{DM}	106	A
Maximum Power Dissipation*	P_D	$T_C=25^\circ C$	28
		$T_C=70^\circ C$	18
		$T_A=25^\circ C$	3
		$T_A=70^\circ C$	2
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	2.6	$^\circ C/W$
Junction-to-Ambient Thermal Resistance*	$R_{\theta JA}$	45	$^\circ C/W$

* The device mounted on $1in^2$ FR4 board with 2 oz copper

* Chip silicon limitation current is 100A

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Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	100			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1		3	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance ^a	$V_{GS}=10V, I_D=20A$		8.5	10.5	m Ω
		$V_{GS}=4.5V, I_D=20A$		12.5	16.5	
V_{SD}	Diode Forward Voltage	$I_S=1A, V_{GS}=0V$			1	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_D=20A$		49.2		nC
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=4.5V, I_D=20A$		26.8		
Q_{gs}	Gate-Source Charge			16		
Q_{gd}	Gate-Drain Charge			10.3		
C_{iss}	Input capacitance	$V_{DS}=30V, V_{GS}=0V, f=1.0MHz$		2819		pF
C_{oss}	Output Capacitance			868		
C_{rss}	Reverse Transfer Capacitance			55		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=50V, R_L=2.5\ \Omega$ $V_{GS}=10V, R_G=6\ \Omega$ $I_D=20A$		25.9		ns
t_r	Turn-On Rise Time			69.5		
$t_{d(off)}$	Turn-Off Delay Time			57.2		
t_f	Turn-Off Fall Time			24		
Single pulse Avalanche Energy						
Single pulse Avalanche Energy $L=0.1mH$		I_{AS}		30		A
Single pulse Avalanche Energy $L=0.1mH$		E_{AS}		45		mJ

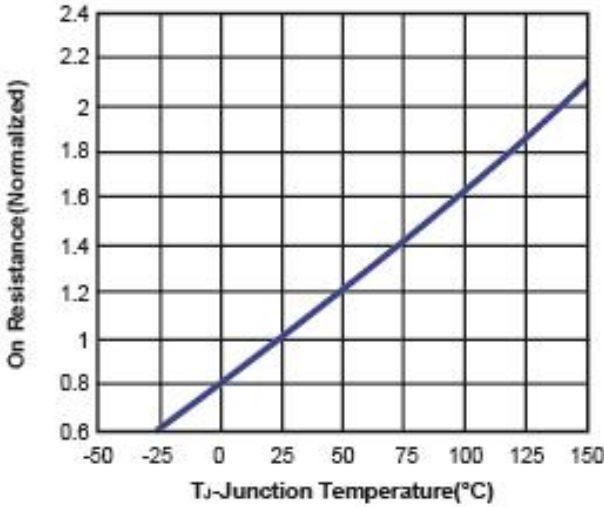
Notes: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

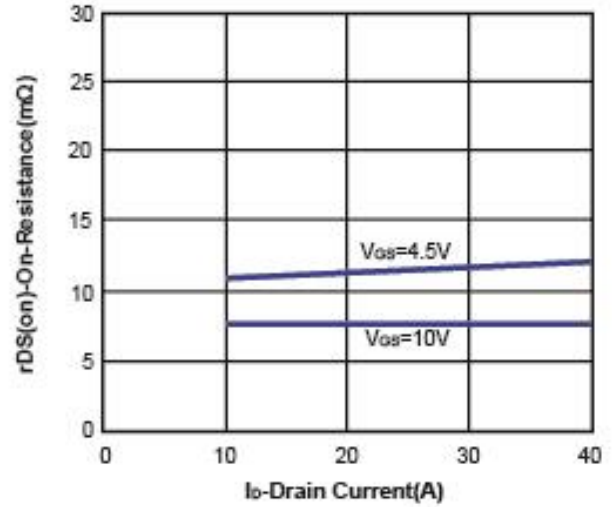


Typical Characteristics (T_J = 25°C Noted)

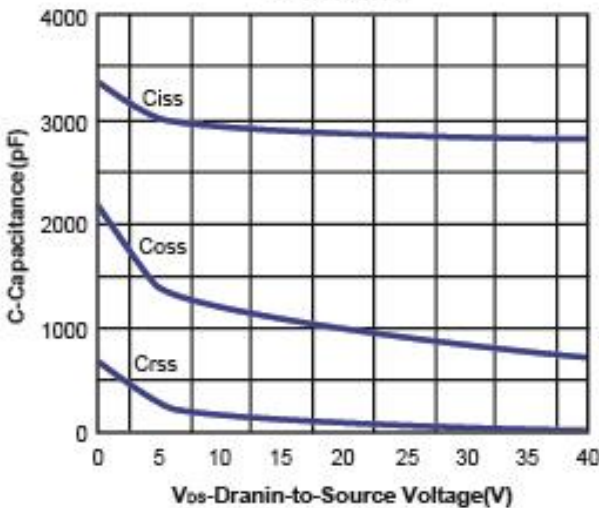
On Resistance vs. Junction Temperature



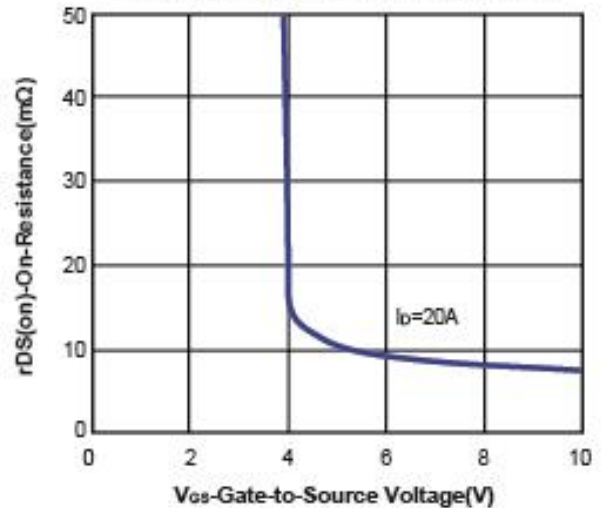
On Resistance vs. Drain Current



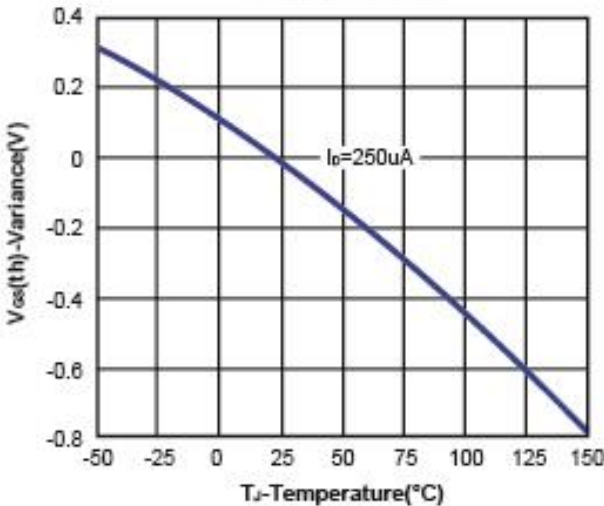
Capacitance



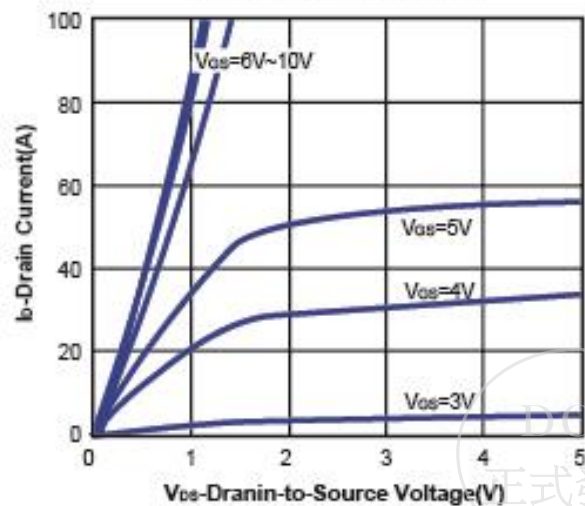
On Resistance vs. Gate-to-Source Voltage



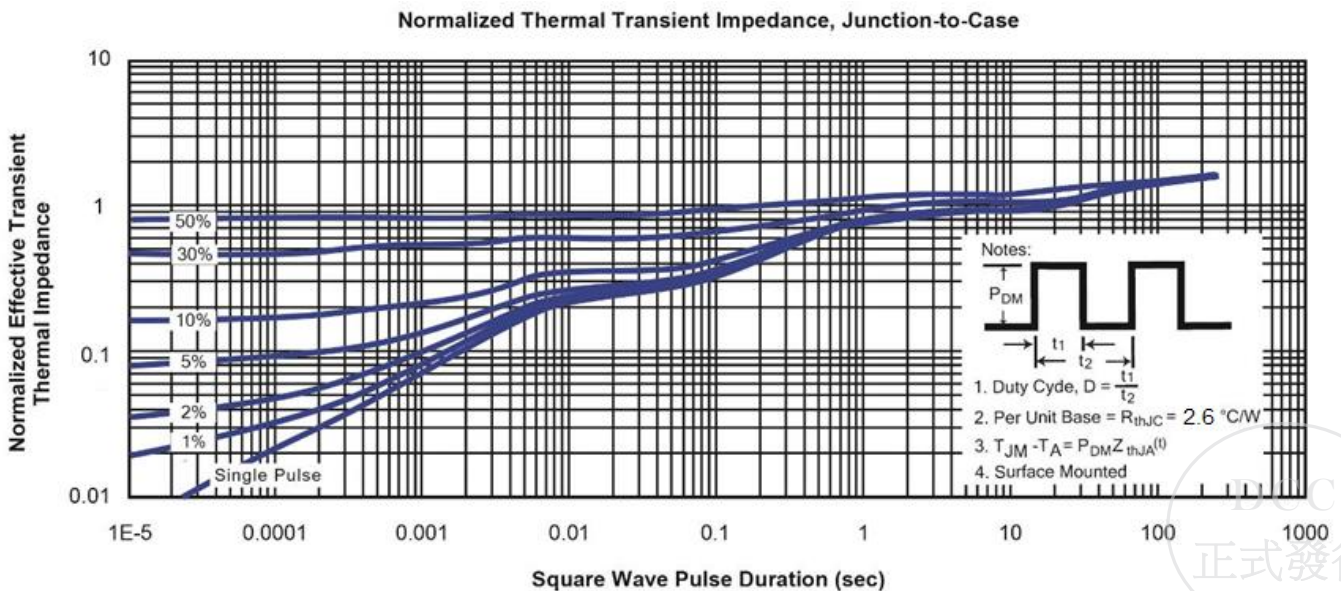
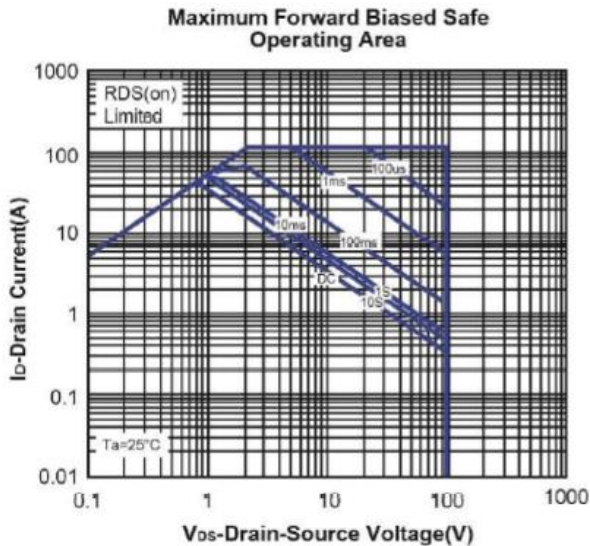
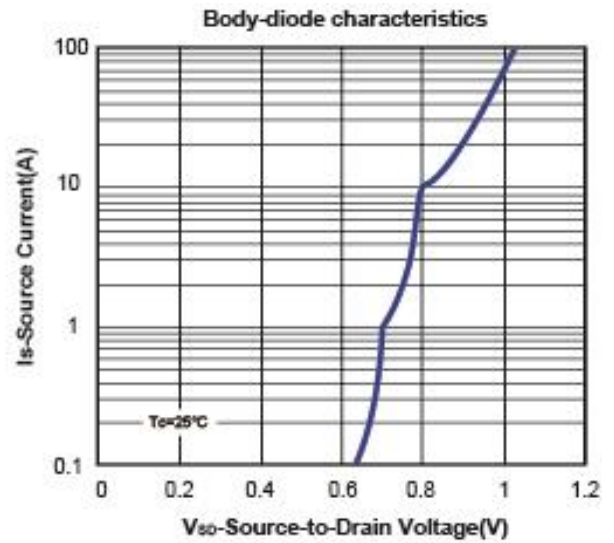
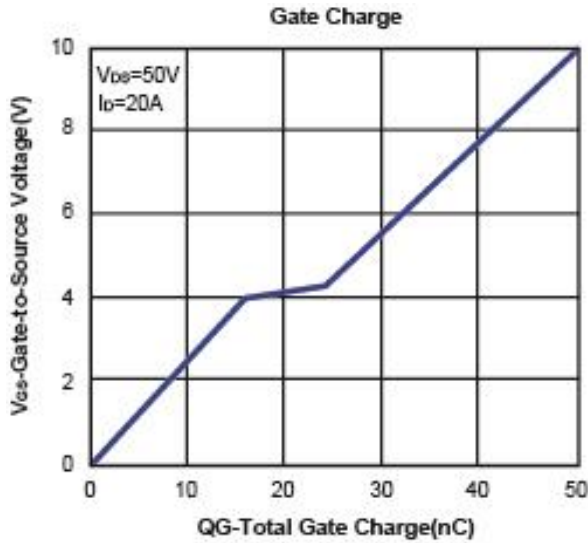
Threshold Voltage



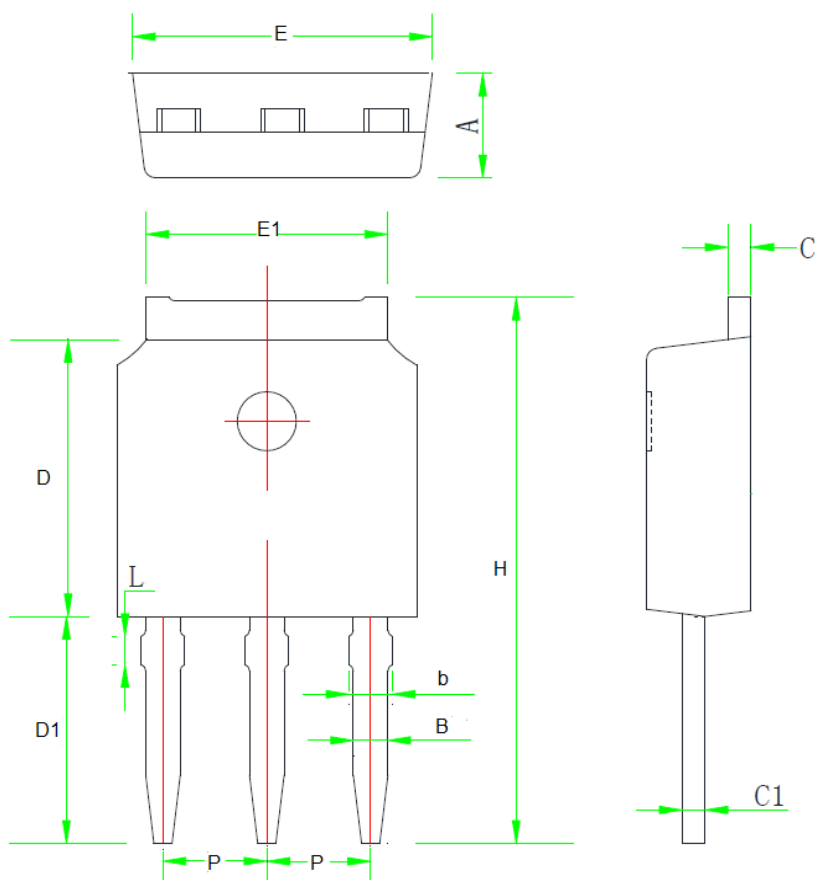
On-Region Characteristics



Typical Characteristics (T_J = 25°C Noted)



TO-251 Package Outline



SYMBOL	MILLIMETERS(mm)	
	MIN	MAX
A	2.00	2.60
B	0.40	0.91
b	0.65	1.15
C	0.35	0.66
C1	0.35	0.67
D	5.30	6.50
D1	3.30	5.50
H	10.20	12.62
E	6.30	6.90
E1	4.80	5.64
L	0.6 BSC	
P	2.30 BSC	

